In the Claims

Please amend the claims as follows:

1. (Currently Amended) A method of testing the routing circuitry in a field programmable gate array (FPGA) comprising:

defining a set of test inputs for a routed network ~~for~~ of a logic circuit;

determining an expected output result for said set of test inputs;

obtaining an actual result by applying said set of test inputs to said routed network~~s~~;

comparing ~~the~~ said expected result with ~~the~~ said actual result; and

A1 flagging ~~the~~ an error if ~~the~~ said expected result is not identical with ~~the~~ said actual result.

2. (Currently Amended) A method of testing ~~the~~ a routing structure in an field programmable gate array (FPGA), said routing structure having a first set of tracks having first and second ends, and a second set of tracks having first and second ends perpendicular to said first set of tracks, said second set of tracks used to route the internal signals of the FPGA, said routing structure having programmable interconnect elements at selected ones of said intersections of said first set of tracks and said second set of tracks comprising:

providing a global control signal to said first end of said first set of tracks that turns on all interconnect elements of said first set of tracks simultaneously;

providing a plurality of signal sources to ~~a~~ said first end of said first set of tracks;

providing a circuit at said second end of said first set of tracks, said circuits producing expected output values in response to selected input stimuli; and

flagging ~~the~~ an error if said expected output values in response to selected input stimuli are not identical with actual values.

3. (Currently Amended) A method of testing ~~the~~ a routing structure in an field programmable gate array (FPGA), said routing structure having a first set of tracks having first and second ends and a second set of tracks having first and second ends perpendicular to said first set of tracks, said second set of tracks used to route the internal signals of the FPGA, said routing structure having programmable interconnect elements at selected ones of said intersections of said first set of tracks and said second set of tracks comprising:

providing a global control signal to said first end of said second set of tracks that turns on all interconnect elements of said second set of tracks simultaneously;

providing a plurality of signal sources to said first end of said second set of tracks;

providing a circuit at said second end of said second set of tracks, said circuits producing expected output values in response to selected input stimuli; and

flagging ~~the~~ an error if said expected output values in response to selected input stimuli are not identical with actual values.

4. (Currently Amended) A method of testing ~~the~~ a routing structure in an field programmable gate array (FPGA), said routing structure having horizontal tracks having first and second ends and vertical tracks having first and second ends used to route the internal signals of the FPGA, said routing structure having programmable interconnect elements at selected ones of said intersections of said horizontal and vertical tracks comprising:

providing a global control signal to said first end of said vertical tracks that turns on all interconnect elements of said vertical tracks simultaneously;

providing a plurality of signal sources to a first end of said vertical tracks;

providing a NOR circuit and a NAND circuit at said second end of said vertical tracks, said circuits producing expected output values in response to selected input stimuli; and

flagging ~~the~~ an error if said expected output values in response to selected input stimuli are not identical with actual values.

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5. (Currently Amended) A method of testing ~~the~~ said routing circuitry in an field programmable gate array (FPGA) according to claim 2 wherein the method of testing the routing circuitry further comprises:

providing a global control signal to said first end of said horizontal tracks that turns all interconnect elements of said horizontal tracks simultaneously;

providing a plurality of signal sources to a first end of said horizontal tracks;

providing a NOR circuit and a NAND circuit at said second end of said horizontal tracks, said circuits producing expected output values; and

flagging ~~the~~ an error if said expected output values are not obtained.